A HIGH-EFFICIENCY SWITCHING POWER SUPPLY

by

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Submitted in Partial Fulfillment

of the Requirements for the

Degree of Bachelor of Science

at the

Massachusetts Institute of Technology

May, 1981

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TABLE OF CONTENTS

TABLES AND FIGURES

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Abstract

My project was to design a switching power supply which output 5 volts regulated at up to about 5 amps load current, given dc inputs of 16 to 60 volts. The circuit I was originally given, which was not working correctly, used a monolithic "switching power supply regulator" chip. I redesigned the switching power supply so that it would work. The original circuit used the switching regulator mentioned above as most of its control section; I discovered that this version of the switching power supply could not work correctly, and redesigned it so that it would. The new control section was formed of discrete components and a pulse-width modulator (PWM). The specifications for this new design were: efficiency >96% (to prevent excessive heat losses), small size, about 7 volts unregulated output (i.e., the ripple is unimportant) with up to 5% variation for loads of 0 to 5 amps, inputs of 10.0 to 40.0 volts, and operating temperature range of -25 to +125 degrees centigrade. These specifications were eventually met.

Theory of Operation

A switching power supply is a dc to dc converter. It accepts a large range of input voltages and outputs a constant dc voltage. It works as diagrammed below in figure 1.

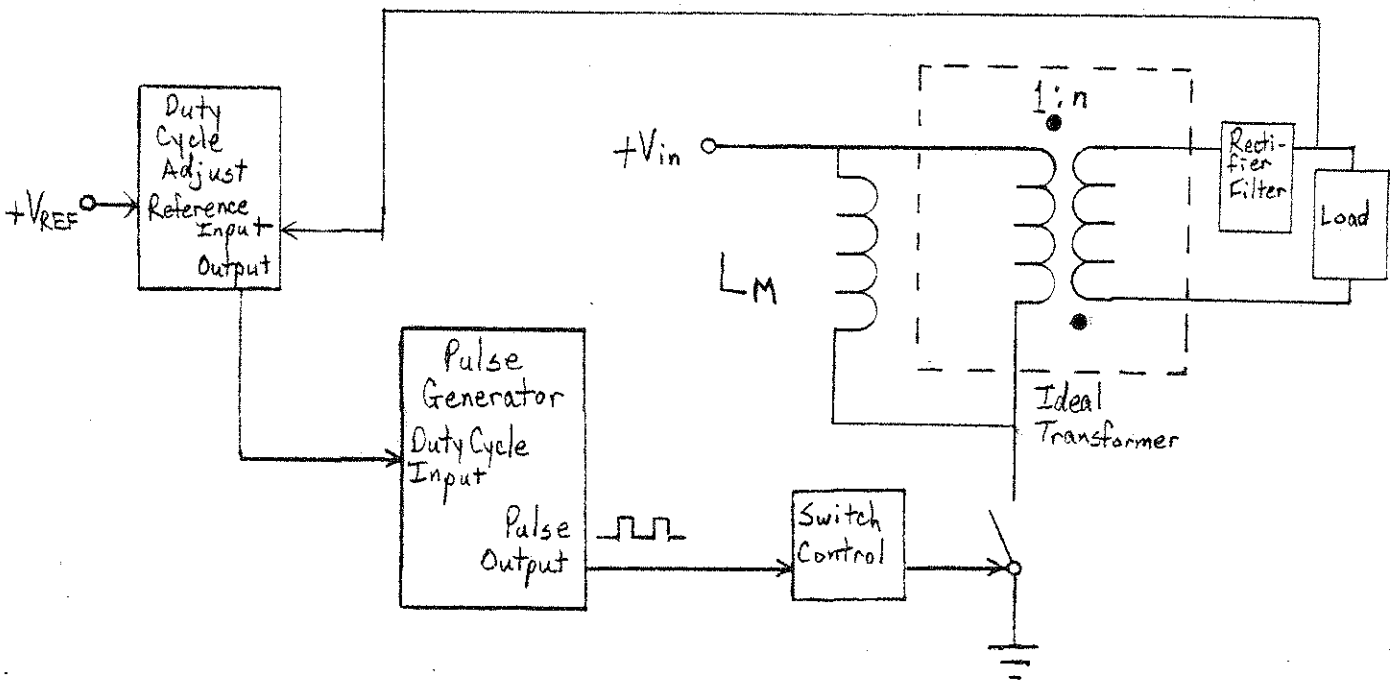


Figure 1: Block Diagram of Switching Power Supply

The pulse generator supplies a pulse train to control the switch. The switch is open when the pulse is low and closed when the pulse is high. The duty cycle of the pulse, that is, the percentage of one period during

which the pulse is high, is represented by D. Then, if the turns ratio of the transformer is 1:n, the voltage transfer ratio is $V_{out}/V_{in}=nD/(1-D)$.

The duty cycle is controlled by some sort of pulse-width modulator (PWM) or other regulator chip. It compares the output voltage with the desired voltage and sets the duty cycle of the pulse such that the dc average of the output should be the desired voltage.

This topology (primary and secondary transformer coils having opposite polarity) is called the "flyback" design. When the switch is closed, current can only pass through the magnetizing inductance of the primary, L_M; the diode is in reverse bias as the voltage across it is $-(V_{out}+V_{in})$. When the switch is opened, current must continue to flow through this inductance (because there is no infinite impulse of voltage), so it passes through the ideal transformer. This current passes through the diode which must then be in forward bias. This charges the capacitor, which supplies power to the load.

There are some important losses in this circuit. There are losses due to eddy currents in the transformer, losses due to coil impedance, losses due to switching impedance, etc. These losses are all due to the fact that the circuit is non-ideal; if we had ideal components, we could theoretically have a power supply with 100% efficiency.

Original Circuit

The circuit is shown below in figure 2.

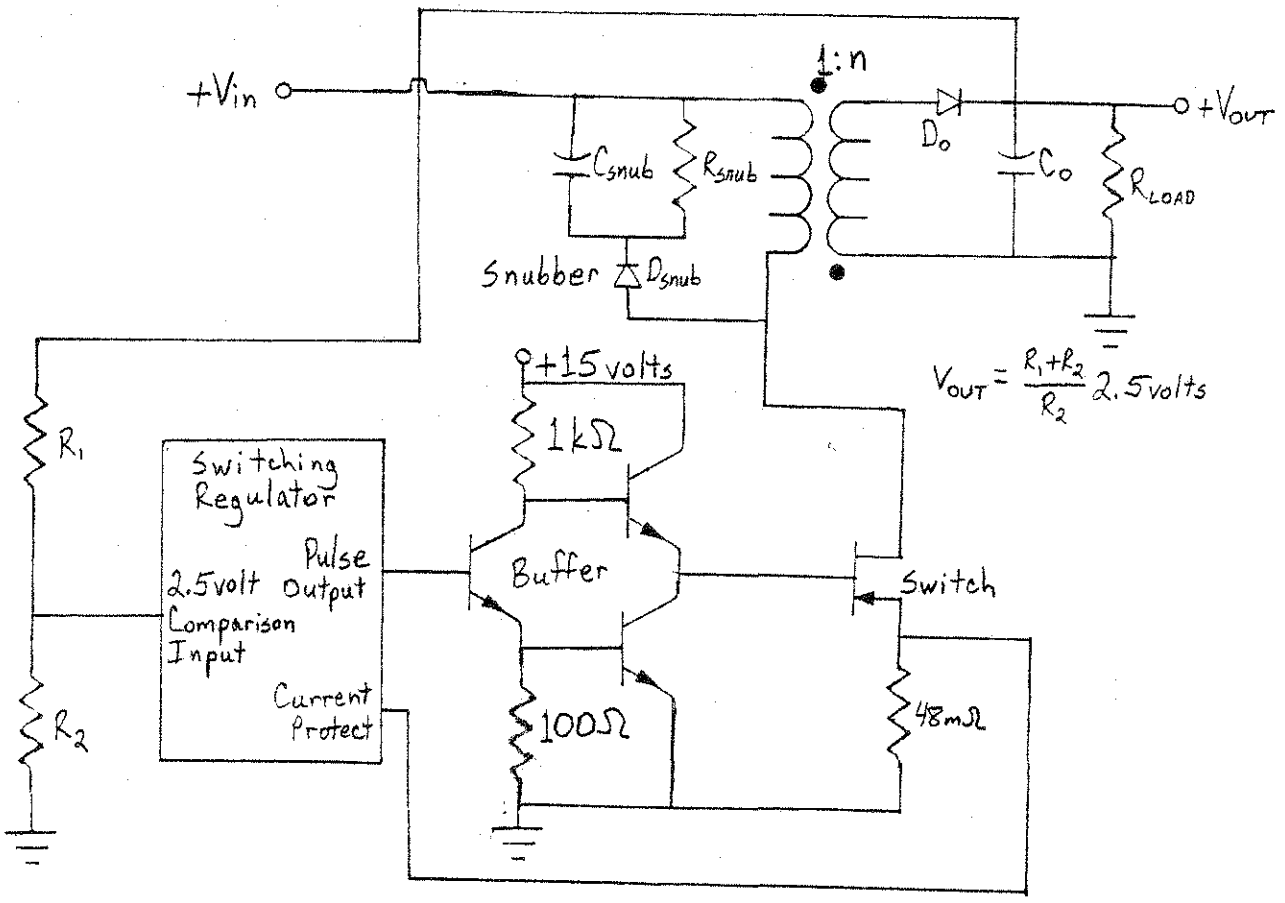


Figure 2: Original Circuit

When this circuit is in operation, a pulse is output to the gate of the field-effect transistor (FET). The width of this pulse is controlled by the switching regulator chip, and is determined by the present output voltage. The frequency of these pulses is 50 kilohertz. When the output, after being scaled by a voltage divider, is larger than the operator-set reference voltage, the pulse is not sent; otherwise, the width of the pulse is set by the difference between this scaled output and the reference. In this circuit, the reference is set by the chip at 2.5 volts, so the output voltage is set at $V_{out}=(2.5 \text{ volts})(R_1+R_2)/R_2$.

The difference between the scaled output voltage and the set reference determines the duty cycle of the pulse. The duty cycle can be as large as 45%, or as small as 0%. The gate-to-source voltage needed to provide saturation of the FET is about 5 volts, so the pulse is passed through a totem-pole style buffer to make sure that the limits of the pulse are about 0 and 15 volts.

When the FET (which is being used as a switch) is "on" its resistance is virtually zero, so essentially all the input voltage appears across the transformer. This transformer is set up in a "flyback" design, as can be seen from figure 2. Thus, while the FET is "on", all the current is passing through the primary, and the power represented by it is being stored in the magnetizing inductance. When the FET turns "off", all the power stored by the magnetizing inductance is released, and this charges the output capacitor.

In the final circuit there was to be a 5 volt regulator at the output, but the circuit I worked on does not have this regulator. My circuit has an unregulated output of approximately 7 volts. Between the primary coil and ground there is a very small resistor, which is used to sense the current through the coil. When the voltage across this resistor grows larger than .48 volt, the system is shut down in order to prevent saturation of the primary coil. When the system is shut down in this manner, it must be completely restarted, which takes several pulse cycles. Since the saturation point of this coil is at least 10 amps, I set

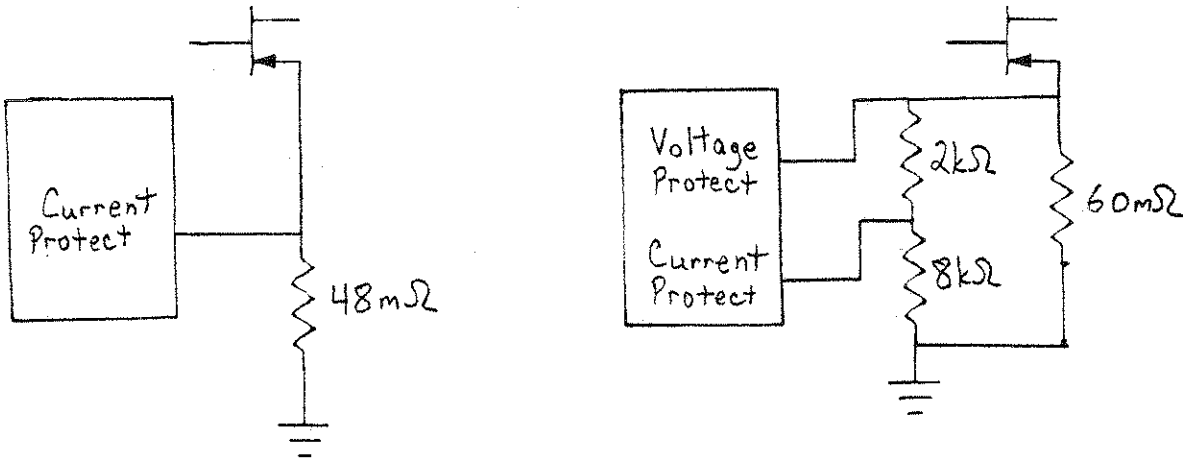
the resistor to be R=V/I=(.48 volt)/(10 amps)=48 milliohms.

There is also a protection circuit to be used if the output voltage is too large; it merely inhibits the next pulse of the pulse generator, and does not shut down the circuit. It can be used as a safety measure to, for example, compare the output voltage with 8 volts and inhibit pulses unless the output is less than this. The difference between this operation and the inhibition inherent in the regulator chip is that this protection circuit turns the pulse off immediately, as well as preventing the next pulse, whereas the regulator section of the chip would merely inhibit the next pulse. A snubber circuit was also added between the FET and the input voltage to protect the FET against short, high voltage spikes due to the impulse of voltage caused by sudden changes in the current through the transformer.

Testing of Original Circuit

Upon testing the circuit, I found that the FET's often failed due to high drain-to-source voltages. This implied that the snubber was not operating effecitvely. I solved this problem by using a larger capacitor in the snubber circuit, thus increasing the amount of charge the snubber can absorb for a given voltage. At this point the circuit worked well for inputs up to about 35 volts, but the output voltage dropped considerably for voltages any larger than this. This was due to the current protection circuit shutting down the system; my first try at a solution was to add a 60 milliohm resistor between the FET and ground, and

connect this to the "voltage too high" prevention section, which cut in at .60 volt. Instead of the 48 milliohm resistor used to sense the voltage for the current protection circuit, I connected a 10 kilohm potentiometer across the 60 milliohm resistor, and adjusted the output to the current protection circuit so that it was .48 volt when the voltage at the voltage protection circuit sensor was .60 volt. This is shown below in figure 3. The idea was to retain the saturation protection of the "current too large" shutdown circuit, while preventing it from operating as often as it did originally.



Original Circuit With Voltage Protect

Figure 3: Protection Circuits

This did not work either; the problem was that the delay between the voltage protect voltage reaching .60 volt and shutdown was .41 microseconds, while the propagation delay for current protection

shutdown was only .16 microseconds. To attempt to circumvent this problem, I disconnected the current protection circuit, but then there was no short circuit or saturation prevention protection, only single-cycle shutdown protection. This was not acceptable from a safety standpoint. Next I tried keeping the current protection intact, but increased the resistance for the voltage protection, so that it would shut down before the current protection caused a complete shutdown. This did not work because, in order to avoid current protection shutdown, the voltage protection shutdown would occur at too low a primary current, so I still could not get the output to be constant. Thus I decided that the circuit, as it was presently designed, could not meet the necessary specifications.

Final Circuit

My final circuit is diagrammed below in figure 4. The main difference between this circuit and the original circuit is that the only monlithic chip used by the final circuit is a PWM. The final circuit works in much the same way as the original one. There are a few differences between the PWM and the switching regulator circuits. The most important ones are:

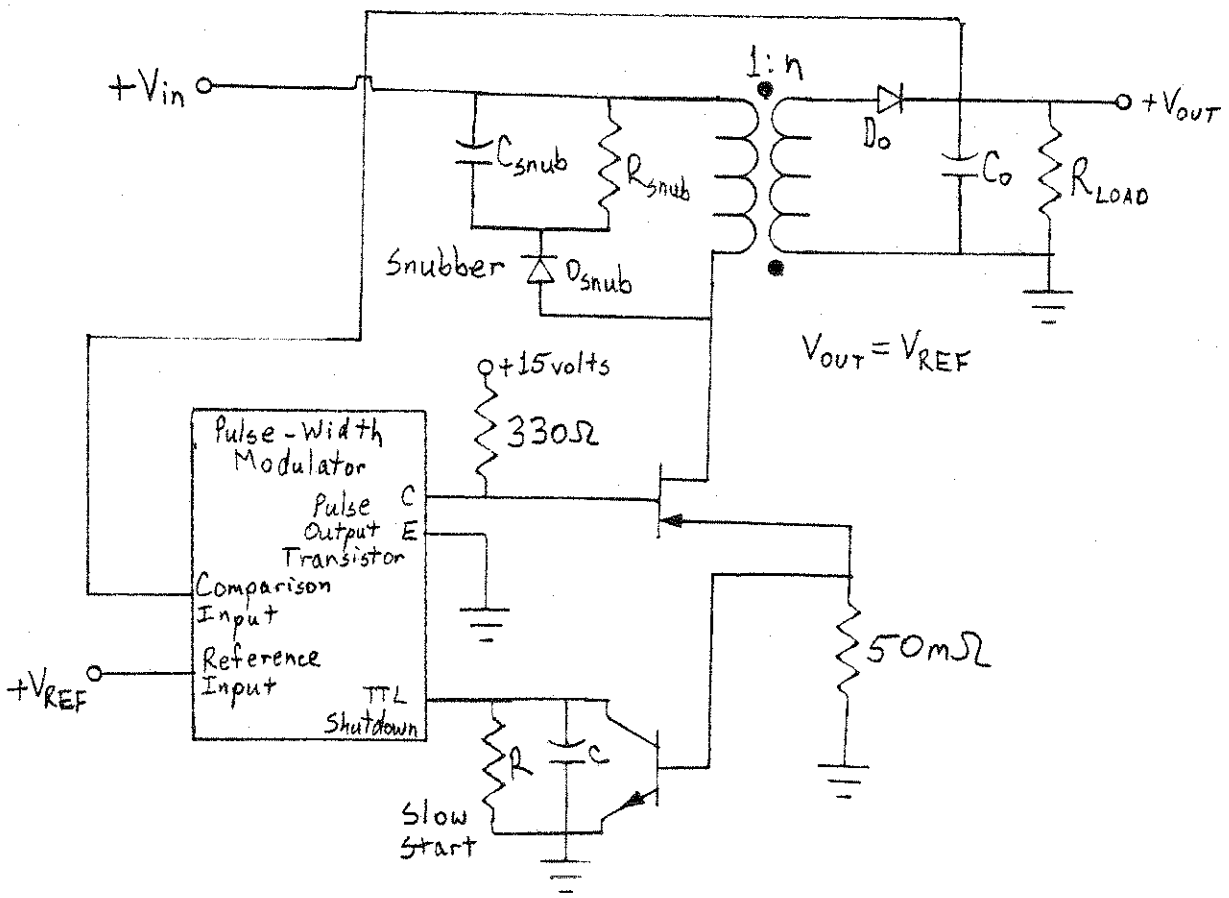


Figure 4: Final Circuit

1) The PWM has a settable comparison voltage for the width-setting comparator, allowing a finer and more accurate adjustment for the output voltage.
2) The PWM has two output transistors, both of reasonable power, driven 180 degrees out of phase, so the need for the buffer is eliminated.
3) The output transistors of the PWM have both collector and emitter availble, supplying a greater degree of freedom to the designer as to what form of switch

is to be used.

4) The PWM has both "current too low" and "current too high" protection circuits, allowing a more accurate adjustment of the current through the primary.

5) The switching regulator has a much better start-up protection circuit, called a slow start function. This keeps the outputs of the chip from starting until all inputs are settled. To have this function on the PWM, I needed to add external circuitry.

6) The PWM has no short circuit protection, i.e., no complete shutdown for current too high. This also required external circuitry to fix.

7) The PWM has no voltage protection circuit, which was not important because I didn't use it in either the original circuit or this one.

8) The switching regulator had a maximum duty cycle adjustment, so I could have changed the minimum input voltage with the original circuit. This was not at all important, since I set the maximum duty cycle for 45% in the original circuit, and it was forced to 45% by the PWM.

9) Since the PWM requires external circuitry, the final circuit is larger than the original.

10) The PWM has a TTL compatible shutdown circuit,

which shuts down the circuit if an element attached to it draws at least 200 microamps.

The only major problem here is 9), and that can be circumvented by proper design technique. The required final size of the circuit is less than 4"X4"X2", which I was able to meet.

The external circuitry needed for the short circuit shutdown was quite simple, and included the "slow start" protection desired. Between the FET and ground I connected a small resistor, about 50 milliohms, and connected the high end of that to the base of a bipolar transistor. The collector of this transistor was connected to the TTL shutdown of the PWM, as well as to ground through a parallel combination of a resistor and capacitor. When the voltage at the base of the transistor grew larger than about .50 volt, it would draw more than 200 microamps, and shut down the circuit. Then, to restart the circuit, the capacitor had to be charged to nearly full charge before it stopped drawing 200 microamps and allowed the circuit to restart. This charging time turned out to be on the order of the RC time constant of this subcircuit. When there were short, high current peaks, the transistor would only be on a short time, so the capacitor would not discharge much and the circuit would only shut down for about one cycle. This worked much the same as the voltage protection circuit of the switching regulator. On the other hand, if the current remained high, as in a short circuit or a saturation condition, the capacitor was entirely discharged, and the "slow start" situation would occur. Thus, the final circuit had all the necessary

functions of the original one.

Testing of Final Circuit

Testing revealed the following about the circuit:

Output voltage was constant while running for five hours without being turned off.

Voltage varied less than 1% for -25 to +125 degrees centigrade ambient temperature.

Circuit size was 4"X4"X1".

Efficiency was about 98%.

Output varied less than 0.8% for load currents of 0 to 6 amps.

Average output voltage during testing period was 7.39 volts.

All protection circuits worked correctly.

Table 1: Tests of Final Circuit

V_{in}, volts	V_{out}, volts	% from average
10.0	7.26	-1.74
15.0	7.33	-0.80
20.0	7.35	-0.52
25.0	7.37	-0.25
30.0	7.43	+0.56
35.0	7.46	+0.96
37.0	7.41	+0.29
40.0	7.50	+1.51

The drop in % difference from average at 37.0 volts is due to the PWM turning off the pulse for one cycle.

Conclusions

The circuit successfully met all requirements. The unresolved questions remaining are:

1) Is there any way to make the circuit smaller?
2) Is there any way to make the circuit run more efficiently, or cooler?
3) What is the projected lifetime of this circuit?

These questions still remained when my work on this project was finished. The only way to answer them would be to do more work on it.